Course Outline for Electronic Systems Technology 55B

DIGITAL LOGIC SYSTEMS

Catalog Description:

ESYS 55B - Digital Logic Systems 2.00 units

Architecture, programming, application and troubleshooting of complex programmable logic device (CPLD) electronic systems. Includes programming in VHDL. Digital building blocks, number systems, Boolean algebra, combinational and sequential logic, integrated logic families, digital circuit measurement techniques and instrumentation, troubleshooting techniques.

Strongly Recommended: ESYS 55A

Grading Option: Letter Grade

Discipline:

<table>
<thead>
<tr>
<th>Units</th>
<th>Contact Hours</th>
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<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Lecture</td>
<td>1</td>
</tr>
<tr>
<td>Laboratory</td>
<td>2</td>
</tr>
<tr>
<td>Clinical</td>
<td>0.00</td>
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<tr>
<td>Total</td>
<td>2.00</td>
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Prerequisite Skills:

None

Measurable Objectives:

Upon completion of this course, the student should be able to:
1. trace timing and control signals with appropriate test equipment and schematic diagrams;
2. program in VHDL for diagnostics purposes;
3. interpret manufacturers’ data sheets for CPLD devices;
4. use test equipment to troubleshoot digital electronic systems;
5. analyze the operation of digital logic systems;
6. apply binary, octal, decimal and hexadecimal numbering systems to digital systems.

Course Content:

1. Course Content, Lecture:
   A. Logic functions and gates
   B. Boolean algebra and combinational logic
   C. Introduction to CPLDs
   D. Combinational logic functions
   E. Digital arithmetic and arithmetic circuits
   F. Sequential logic
   G. PAL architectures
   H. Counters and shift registers
   I. State machine design
   J. Logic gate circuitry

2. Course Content, Laboratory:
   A. Logic functions and gates
   B. Boolean algebra and combinational logic
   C. Introduction to CPLDs
   D. Combinational logic functions
   E. Digital arithmetic and arithmetic circuits
   F. Sequential logic
   G. Counters and shift registers
   H. State machine design
   I. Logic gate circuitry

Methods of Presentation

1. Lecture/Discussion
2. Laboratory
3. Online learning objects

Assignments and Methods of Evaluating Student Progress

1. Typical Assignments
   A. Analyze the functions of a CPLD logic circuit with graphic gate design.
   B. Manually solve digital arithmetic problems and verify the result with the arithmetic function implemented in VHDL.

2. Methods of Evaluating Student Progress
   A. Exams/Tests
   B. Quizzes
   C. Papers
3. Student Learning Outcomes
Upon the completion of this course, the student should be able to:
A. The student will identify basic digital logic elements and analyze the operation of digital logic circuits in simulations and FPGA implementations.
B. The student will use standard test equipment, system documentation, logic diagrams, and VHDL listings to measure and verify timing, inputs, and outputs of a given basic logic circuit implemented in an FPGA.

Textbook (Typical):
1. Lessons in Electric Circuits, Vol. 4, 2015, Kuphaldt, T., open source, hosted on ibiblio.org

Special Student Materials
Abbreviated Class Schedule Description:
Architecture, programming, application and troubleshooting of complex programmable logic device (CPLD) electronic systems. Includes programming in VHDL. Digital building blocks, number systems, Boolean algebra, combinational and sequential logic, integrated logic families, digital circuit measurement techniques and instrumentation, troubleshooting techniques.

Strongly Recommended: ESYS 55A